List of Claims:

Claims 1-7 (cancelled)

Claim 8 (currently amended): A memory cell comprising:

a semiconductor substrate having a first region and a second region of one conduction type and a third region therebetween of an opposite conduction type;

a gate insulating layer situated over ~~said substrate~~ an entire length of said third region and substantially less than an entire length of each of said first region and said second region, the gate insulating layer having a first thickness situated over said first region and said second region, and a second thickness situated over said third region, said first thickness being greater than said second thickness, wherein said first thickness is substantially uniform and said second thickness is substantially uniform; and

a control gate situated over said gate insulating layer.

Claim 9 (currently amended): A memory cell comprising:

a semiconductor substrate having a first region and a second region of one conduction type and a third region therebetween of an opposite conduction type; and

a gate insulating layer situated over ~~said substrate~~ an entire length of said third region and substantially less than an entire length of each of said first region and said second region, the gate insulating layer having a first thickness situated over said first region and said second region, and a second thickness situated over said third region, said first thickness being greater than said second thickness, wherein said first thickness is substantially uniform and said second thickness is substantially uniform; and

an ONO stack situated over said gate insulating layer.

Claims 10-13 (cancelled)

Claim 14 (previously presented): A memory cell as in claim 8, wherein said first thickness is between about 20 and 30 nm and wherein said second thickness is between about 8 and 11 nm.

Claim 15 (previously amended): A memory cell as in claim 8, wherein an injection field in an overlap region situated between said gate insulating layer and said first and second regions ranges between approximately 4 Mv/cm and approximately 6 Mv/cm.

Claim 16 (previously amended): A memory cell as in claim 8, wherein an injection field in an overlap region situated between said gate insulating layer and said third region ranges between approximately 8 Mv/cm and approximately 11 Mv/cm.

Claim 17 (previously presented): A memory cell as in claim 8, wherein said gate insulating layer comprises SiO_2.

Claim 18 (cancelled)

Claim 19 (previously presented): A memory cell as in claim 9, wherein said first thickness is between about 20 and 30 nm and wherein said second thickness is between about 8 and 11 nm.

Claim 20 (previously amended): A memory cell as in claim 9, wherein an injection field in an overlap region situated between said gate insulating layer and said

first and second regions ranges between approximately 4 Mv/cm and approximately 6 Mv/cm.

Claim 21 (previously amended): A memory cell as in claim 9, wherein an injection field in an overlap region situated between said gate insulating layer and said third region ranges between approximately 8 Mv/cm and approximately 11 Mv/cm.

Claim 22 (previously presented): A memory cell as in claim 9, wherein said gate insulating layer comprises SiO_2.